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(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Fuller et al.

Application No.: 10/081,624 | Confirmation No.: 1950

Filed: February 20, 2002 | Art Unit: 1733

For: MICROELECTRONIC DEVICE HAVING A PLURALITY OF STACKED DIES AND METHODS FOR MANUFACTURING SUCH MICROELECTRONIC ASSEMBLIES | Examiner: J. Rossi

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This brief is in furtherance of the Notice of Appeal in this case filed on March 13, 2006. The fees required under § 41.20(b)(2), and a petition for an extension of time and the associated fee, are addressed in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and MPEP § 1206:

Appendix B Evidence

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is Micron Technology, Inc.

II. RELATED APPEALS, INTERFERENCES, AND JUDICIAL PROCEEDINGS

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 12 claims pending in this application.

B. Current Status of Claims

1. Claims canceled: 3-7 and 12-47
2. Claims withdrawn from consideration but not canceled: none
3. Claims pending: 1, 2, 8-11 and 48-53
4. Claims allowed: none
5. Claims rejected: 1, 2, 8-11 and 48-53

C. Claims on Appeal

Claims 1, 2, 8-11 and 48-53 are on appeal.

IV. STATUS OF AMENDMENTS

A Response was filed on February 13, 2006, after issuance of the Final Office Action mailed on October 12, 2005. No claims were added, amended, or cancelled in the February 13 Response.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Many electrical products require packaged microelectronic devices to have an extremely high density of components in a very limited amount of space. (*See, e.g.,* Specification, 2:12-13.) For example, the space available for memory devices, processors, displays and other microelectronic components is quite limited in cell phones, personal digital assistants, portable computers and many other products. (*See, e.g.,* Specification, 2:13-16.) As such, there is a strong drive to reduce the "footprint" and/or the height of packaged microelectronic devices. (*See, e.g.,* Specification, 2:16-18.)

One technique to increase the density of microelectronic devices within a footprint on a printed circuit board is to stack one microelectronic die on top of another. (*See, e.g.,* Specification, 2:22-24.) It will be appreciated that stacking the dies increases the density of microelectronic devices within a given footprint. (*See, e.g.,* Specification, 2:24-25.) The microelectronic dies are typically stacked on each other in a two-pass process starting with a first pass that mounts a flip-chip die to a substrate and a second pass that mounts a conventional wire-bond die onto the backside of the flip-chip die. (*See, e.g.,* Specification, 2:25-28.) The first pass typically involves mounting the flip-chip die to the substrate in a first die attach machine, and then heating the die/substrate subassembly to reflow the solder bumps between the die and substrate. (*See, e.g.,* Specification, 2:28-3:1.) This heating process securely attaches the flip-chip die to the substrate. (*See, e.g.,* Specification, 3:1.) After mounting the flip-chip die to the substrate, the die/substrate subassembly is transported to a second die attach machine where it is held for processing in a second-pass. (*See, e.g.,* Specification, 3:2-4.) The second pass through the second die attach machine involves (a) dispensing epoxy onto the backside of the flip-chip die, and (b) mounting a conventional wire-bond die to the epoxy. (*See, e.g.,* Specification, 3:4-6.) The stacked die assembly is then re-heated to

cure the epoxy after the second pass through the second die attach machine. (*See, e.g.,* Specification, 3:6-8.)

Many conventional two-pass processes for stacking a wire-bond die onto the backside of a flip-chip die typically occur in two different die attach machines. (*See, e.g.,* Specification, 3:9-11.) Other two-pass processes can also occur in a single die attach machine by mounting the flip-chip die to the substrate in a first pass, heating the mounted flip-chip die in a first heating cycle to reflow the solder on the flip-chip die, reprogramming the die attach machine to attach the wire-bond die to the backside of the mounted flip-chip die in a separate second-pass through the machine, attaching the wire-bond die to an epoxy on the flip-chip die in a second pass through the same die attach machine, reheating the stacked die assembly, and then reprogramming the die attach machine again to mount a flip-chip die to another substrate in a new first pass. (*See, e.g.,* Specification, 3:11-19.)

One problem associated with the two-pass procedures for stacking dies is that they inefficiently handle the dies and reduce the throughput of packaged devices. (*See, e.g.,* Specification, 3:20-21.) A two-pass system inherently requires a large number of substrates and flip-chip dies to be maintained at the front end of the first-pass die attach machine and a large inventory of flip-chip/substrate subassemblies to be held at the second-pass die attach machine. (*See, e.g.,* Specification, 3:22-25.) Holding a large number of components at various stages of conventional stacking processes reduces the efficiency of these processes. (*See, e.g.,* Specification, 3:25-27.) Therefore, the conventional two-pass procedures for assembling stacked microelectronic dies are inefficient and reduce the throughput of finished products. (*See, e.g.,* Specification, 3:27-29.)

Another problem of the two-pass die attach procedures is that they are expensive to implement and operate. (*See, e.g.,* Specification, 4:1-2.) For example, in applications that use different die attach machines for the first and second passes, a number of machines are accordingly dedicated to each individual operation and a large number of operators are required to run and monitor the individual machines. (*See, e.g.,* Specification, 4:2-5.) As a result, a significant amount of capital is required for purchasing the machines and building the clean facilities for housing these machines. (*See, e.g.,* Specification, 4:5-7.) Moreover, the continuing operating costs for the

personnel to operate such a large number of different machines can also be quite high. (*See, e.g.,* Specification, 4:7-8.) The two-pass procedures that run two separate passes through a single machine are also expensive because they require a significant amount of down time to reprogram the machine to switch back and forth from processing flip-chip dies to processing conventional wire-bond dies. (*See, e.g.,* Specification, 4:9-13.) The down time reduces the throughput and increases the operating cost of using a single die attach machine for performing conventional two-pass procedures. (*See, e.g.,* Specification, 4:13-15.)

A. Claim 1

Several embodiments of the present invention resolve the above-described problems of the two-pass die attach procedures by stacking a second die on a first die before securing the first die to the substrate in a heating cycle. (*See, e.g.,* Specification, 6:29-7:2.) For example, one embodiment of a method for assembling microelectronic dies set forth in claim 1 comprises placing a base die on a substrate in a die attach machine so that a front side of the base die with bond pads faces toward the substrate and a backside of the base die faces away from the substrate. (*See, e.g.,* Specification, 8:21-23.) The method further includes stacking a first stacked die onto the backside of the base die in the same die attach machine by dispensing an adhesive onto the backside of the base die and placing a backside of the first stacked die onto the adhesive. (*See, e.g.,* Specification, 8:27-9:5.) The first stacked die is stacked onto the base die before securing the base die to the substrate in a heating cycle. (*See, e.g.,* Specification, 9:5-7.)

B. Claim 10

Another method for assembling microelectronic dies in accordance with an embodiment of the invention set forth in claim 10 comprises preparing a substrate to receive a base die in a die attach machine, placing the base die on the substrate in the die attach machine so that a front side of the base die with bond pads faces toward the substrate and a backside of the base die faces away from the substrate, and moving the base die within the same die attach machine without heating the base die. (*See, e.g.,* Specification, 6:13-17, 8:21-23, and 7:4-7.) The method further includes stacking a first stacked die onto the base die in the die attach machine by dispensing an adhesive

onto the backside of the base die and placing the first stacked die onto the adhesive. (*See, e.g.*, Specification, 8:27-9:5.)

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 2, 8-11 and 48-53 were rejected under 35 U.S.C. § 103(a) over the combination of (a) the information in the Background of the present application ("Background Information"), (b) U.S. Patent No. 6,378,200 to Lim et al. ("Lim"), and (c) U.S. Patent No. 6,071,371 to Leonard et al. ("Leonard").

VII. ARGUMENTS

Claims 1, 2, 8-11 and 48-53 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Background Information in view of Lim and Leonard. "[T]he examiner bears the initial burden of presenting a *prima facie* case of obviousness." *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d, 1955, 1956 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, the Examiner needs to (a) identity prior art references that disclose all the elements of the claims, and (b) provide a suggestion or motivation to combine the references. (MPEP § 2143.) As set forth in detail below, the Examiner has failed to satisfy the burden of presenting a *prima facie* case of obviousness because the combination of the Background Information, Lim and Leonard fails to disclose all the elements of the claims and there is no motivation to combine the references.

A. Claim 1 is Directed to a Method for Assembling Microelectronic Dies Including, *inter alia*, Placing a Base Die on a Substrate and Stacking a First Stacked Die onto the Base Die Before Securing the Base Die to the Substrate in a Heating Cycle

Claim 1 is directed to a method for assembling microelectronic dies including placing a base die on a substrate in a die attach machine so that a front side of the base die with bond pads faces toward the substrate and a backside of the base die faces away from the substrate. The method further includes stacking a first stacked die onto the backside of the base die in the same die attach machine by dispensing an adhesive onto the backside of the base die and placing a backside of the

first stacked die onto the adhesive. The first stacked die is stacked onto the base die before securing the base die to the substrate in a heating cycle.

B. The Background Information Discloses Methods for Stacking Dies on Printed Circuit Boards

The Background Information discloses methods for stacking dies on printed circuit boards. The microelectronic dies are typically stacked on each other in a two-pass process starting with a first pass that mounts a flip-chip die to a substrate and a second pass that mounts a conventional wire-bond die onto the backside of the flip-chip die. "The first pass typically involves mounting the flip-chip die to the substrate in a first die attach machine, and then heating the flip-chip/substrate subassembly to reflow solder bumps" between the die and substrate. (Specification, 2:28-3:1.) This heating process securely attaches the flip-chip die to the substrate. After securing the flip-chip die to the substrate using heat, the die/substrate subassembly is transported to a second die attach machine where it is held for processing in a second-pass. The second pass through the second die attach machine involves (a) dispensing epoxy onto the backside of the flip-chip die, and (b) mounting a conventional wire-bond die to the epoxy. The stacked die assembly is then re-heated to cure the epoxy after the second pass through the second die attach machine.

The conventional two-pass process for stacking a wire-bond die onto the backside of a flip-chip die typically occurs in two different die attach machines. Alternatively, a single die attach machine may be used by mounting the flip-chip die to the substrate in a first pass, heating the mounted flip-chip die in a first heating cycle to reflow the solder on the flip-chip die, reprogramming the die attach machine to attach the wire-bond die to the backside of the mounted flip-chip die in a separate second-pass through the machine, attaching the wire-bond die to an epoxy on the flip-chip die in a second pass through the same die attach machine, reheating the stacked die assembly, and then reprogramming the die attach machine again to mount a flip-chip die to another substrate in a new first pass.

The Background Information also teaches that it is generally necessary to heat the subassembly of the base die and the substrate before moving or otherwise handling the subassembly

to avoid displacing the base die. (Specification, paragraph [0030].) The Background Information further teaches that it was counterintuitive to attach the first stacked die to the base die before securing the base die to the substrate because the first stacked die may displace the unsecured base die and render the device inoperable. (Id.)

C. Lim Discloses a Method of Reconfiguring an Assembly Line for Electronic Products

Lim discloses a method of reconfiguring a production line for fabricating printed circuit board assemblies to achieve maximum efficiency and maximum flexibility. The production line has one or more placement stations, a reflow oven, a conveyer, and a controller. The controller communicates with the placement stations, the reflow oven, and the conveyer to determine the status of these components and adjust the tasks performed by these components. For example, if a first placement station typically performs a first task and a second placement station downstream from the first placement station typically performs a second task, the controller may move a printed circuit board assembly from the first station to the second station and reconfigure the second station to temporarily perform both the first and second tasks when the second station is idle.

D. Leonard Discloses a Method for Simultaneously Attaching Surface Mount and Chip-on-Board Dies Directly to a Circuit Board

Leonard discloses a method for simultaneously attaching both a surface-mount die (i.e., flip-chip die) and a chip-on-board die (i.e., a wire-bond die) to a circuit board. The surface-mount die and the chip-on-board die are both attached directly to the circuit board and laterally spaced apart from each other. The surface-mount die is attached to the circuit board with a solder joint, and the chip-on-board die is attached to the circuit board with an adhesive. After placing the dies on the circuit board, the assembly is heated to cure the adhesive and reflow the solder.

E. The Background Information, Leonard, and Lim Fail to Disclose or Suggest a Method for Assembling Microelectronic Dies Including, *inter alia*, Placing a Base Die on a Substrate and Stacking a First Stacked Die onto the Base Die Before Securing the Base Die to the Substrate in a Heating Cycle

The Background Information, Leonard, and Lim fail to disclose or suggest a method for assembling microelectronic dies including, *intra alia*, "placing a base die on a substrate in a die attach machine" and "stacking a first stacked die onto the backside of the base die in the same die attach machine . . . before securing the base die to the substrate in a heating cycle," as recited in claim 1. In the Advisory Action, the Examiner alleges:

> since the Admitted Prior Art teaches using heat to reflow solder to attach the flip chip to the substrate and using heat to cure an adhesive to attach the wire bond chip to the backside of the flip chip, it would have been obvious to one of ordinary skill in the art to perform one heating step to both reflow the solder and cure the adhesive in order to attach the flip chip to the substrate and attach the wire bond chip to the flip chip, because a single heating step for both reflowing solder and curing adhesive to simultaneously attach chips/dies to a board/substrate is known in the art.

(Advisory Action, pp. 3-4.) The undersigned attorney respectfully disagrees for the reasons described below.

One of ordinary skill in the art would not be motivated to modify the Background Information as suggested by the Examiner because, among other reasons, the Background Information explicitly teaches away from such a modification. Specifically, the Background Information teaches that it is generally necessary to heat the subassembly of the base die and the substrate before moving or otherwise handling the subassembly to avoid displacing the base die. (Specification, paragraph [0030].) The Background Information further teaches that it was counterintuitive to attach the first stacked die to the base die before securing the base die to the substrate because doing so may displace the base die. (Id.) The Background Information accordingly explicitly teaches away from stacking a first stacked die onto the backside of the base die before securing the base die to the substrate in a heating cycle.

In response to the above-noted argument, the Examiner stated:

> [t]he examiner respectfully points out that section [0030] of the present specification is part of Applicant's detailed description of the present invention and NOT the background/admitted prior art, as implied by Applicant in his remarks. The background section of the present specification includes sections [0002-0009] and nowhere in these sections does it ever state that it is generally necessary to heat the subassembly of the base die and the substrate before moving or otherwise handling the subassembly to avoid displacing the base die and/or that it is counterintuitive to attach the first stacked die to the base die before securing the base die to the substrate—such is merely Applicant's own interpretation of the Admitted Prior Art.

(Advisory Action, pp. 2-3.)

The undersigned attorney respectfully disagrees. All of applicants' statements regarding the prior art in the application as originally filed constitute prior art even if the statements appear in the Detailed Description section. MPEP § 2129, states, "[w]hen applicant states that something is prior art, it is taken as being available as prior art." In the present application, the applicants described the prior art in both the Background and Detailed Description sections of the originally-filed application. Specifically, the pertinent portion of paragraph [0030] of the Detailed Description recites, "[u]sing only a single heating stage is counter intuitive to the prior teachings of the art that generally disclose it is necessary to heat the subassembly of the base die and the substrate before moving or otherwise handling the subassembly to avoid displacing the base die." (Emphasis added.) This statement in the Detailed Description section clearly describes the prior art. The Examiner cannot selectively ignore portions of applicants' description of the prior art solely because those portions appear in the Detailed Description. When properly considered the whole of the Background Information explicitly teaches away from stacking a first stacked die onto the backside of the base die before securing the base die to the substrate in a heating cycle.

The law does not allow one reference to be modified to come up with the claimed combination of features when the reasoning for the modification ignores the portion of the reference that teaches away from making the claimed structure. To meet the burden of establishing a *prima facie* case of obviousness, "the Examiner must show that there is either a suggestion in the art to produce the claimed invention or a compelling motivation based on sound scientific principles." *Ex*

parte Kranz, 19 U.S.P.Q.2d 1216, 1218 (Bd. Pat. App. & Interf. 1991). To show such a suggestion, the Examiner must show that "the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). Moreover, a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would teach away from the claimed invention. *W.L. Gore & Assoc., Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 U.S.P.Q. 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). This same standard is echoed in MPEP § 2142:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.

The MPEP goes on to explain that if the references do not "expressly or impliedly suggest the claimed invention," it is the Examiner's burden to "present a convincing line of reasoning" as to why the modification would have been obvious. *Id.* (*quoting Ex Parte Clapp*, 227 U.S.P.Q. 972, 973 (Bd. Pat. App. & Inter. 1985)). This line of reasoning must be more than vague conjecture about *possible* modifications of the prior art.

> The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. . . . Although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so."

MPEP § 2143.01 (*quoting In re Mills*, 916 F.2d 680, 16 U.S.P.Q. 2d 1430 (Fed. Cir. 1990)).

Moreover, Lim and Leonard do not provide a motivation to modify the Background Information to include the claimed combination of features and stack a first stacked die onto the backside of a base die before securing the base die to the substrate in a heating cycle. At best, Lim discloses a method for reassigning tasks to different components in a production line to minimize

inefficiencies in the line, and Leonard discloses a method for simultaneously curing two different materials that attach two laterally spaced-apart dies to the same circuit board. Neither of these references mentions stacking dies or curing adhesive materials that couple stacked dies. In fact, Leonard teaches away from stacking a first stacked die onto the backside of a base die. Specifically, Leonard's primary purpose is to place both a surface-mount die and a chip-on-board die on the printed circuit board, and then simultaneously attach each of the dies directly to the printed circuit board in a heating cycle. As such, Leonard teaches away from the combination of (a) placing a base die on a substrate and (b) subsequently stacking a first stacked die onto the backside of the base die because such a combination would contravene Leonard's primary purpose to place both a surface-mount die and a chip-on-board die directly on the printed circuit board, and then simultaneously attach each of the dies directly to the printed circuit board.

Accordingly, the current rejection of claim 1 does not comply with Section 103(a) because (a) the Background Information expressly teaches away from stacking a first stacked die onto the backside of a base die before securing the base die to the substrate in a heating cycle, and (b) Lim and Leonard do not provide a motivation to modify the Background Information to include this claim feature. Therefore, the Section 103(a) rejection of claim 1 is improper and should be reversed.

Claims 2, 8, 9, 48 and 49 depend from claim 1. Accordingly, the Section 103(a) rejection of claims 2, 8, 9, 48 and 49 is improper and should be reversed for at least the reasons discussed above with reference to claim 1 and for the additional features of these claims.

Independent claim 10 has, *inter alia*, features generally analogous to the features of claim 1. Accordingly, the Section 103(a) rejection of claim 10 is improper and should be reversed for at least the reasons discussed above with reference to claim 1 and for the additional features of claim 10.

Claims 11 and 50-53 depend from claim 10. Accordingly, the Section 103(a) rejection of claims 11 and 50-53 is improper and should be reversed for at least the reasons discussed above with reference to claim 10 and for the additional features of these claims.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A.

IX. EVIDENCE

A copy of the Declarations filed under 37 C.F.R. §§ 1.131 and 1.132 are attached hereto as Appendix B. No other evidence pursuant to §§ 1.130, 1.131, or 1.132 or evidence entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS

No related proceedings are referenced in Section II. above, and no copies of decisions in related proceedings are being provided, hence no Related Proceedings Appendix is included.

Dated: 7/13/06

Respectfully submitted,

By _____

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/081,624

1. (Previously presented) A method for assembling microelectronic dies, comprising:

placing a base die on a substrate in a die attach machine so that a front side of the base die with bond pads faces toward the substrate and a backside of the base die faces away from the substrate; and

stacking a first stacked die onto the backside of the base die in the same die attach machine by dispensing an adhesive onto the backside of the base die and placing a backside of the first stacked die onto the adhesive, wherein the first stacked die is stacked onto the base die before securing the base die to the substrate in a heating cycle.

2. (Previously presented) The method of claim 1, further comprising heating the base die and the first stacked die in a single heating cycle to secure the base die to the substrate and to secure the first stacked die to the base die.

3-7. (Cancelled)

8. (Previously presented) The method of claim 1 wherein placing the base die and stacking the first stacked die occur without loading the substrate and the base die into a separate die attach machine.

9. (Original) The method of claim 1, further comprising placing the base die on the substrate and stacking the first stacked die onto the base die in a single pass through a single die attach machine.

10. (Previously presented) A method for assembling microelectronic dies, comprising:

preparing a substrate to receive a base die in a die attach machine;

placing the base die on the substrate in the die attach machine so that a front side of the base die with bond pads faces toward the substrate and a backside of the base die faces away from the substrate;

moving the base die within the same die attach machine without heating the base die; and

stacking a first stacked die onto the base die in the die attach machine by dispensing an adhesive onto the backside of the base die and placing the first stacked die onto the adhesive.

11. (Original) The method of claim 10, further comprising heating the base die and the first stacked die in a single heating cycle to secure the base die to the substrate and to secure the first stacked die to the base die.

12-47. (Cancelled)

48. (Previously presented) The method of claim 1 wherein placing the base die on the substrate comprises positioning a flip chip on the substrate.

49. (Previously presented) The method of claim 1 wherein dispensing the adhesive onto the backside of the base die comprises depositing an epoxy onto the base die.

50. (Previously presented) The method of claim 10 wherein placing the base die and stacking the first stacked die occur without loading the substrate and the base die into a separate die attach machine.

51. (Previously presented) The method of claim 10 wherein placing the base die on the substrate and stacking the first stacked die onto the base die occur in a single pass through the die attach machine.

52. (Previously presented) The method of claim 10 wherein placing the base die on the substrate comprises positioning a flip chip on the substrate.

53. (Previously presented) The method of claim 10 wherein dispensing the adhesive onto the backside of the base die comprises depositing an epoxy onto the base die.

APPENDIX B

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:	JASON L. FULLER AND SHAUN D. COMPTON	EXAMINER:	JOHN T. HARAN
APPLICATION NO.:	10/081,624	ART UNIT:	1733
FILED:	FEBRUARY 20, 2002	CONF. NO:	1950

FOR: **MICROELECTRONIC DEVICE HAVING A PLURALITY OF STACKED DIES AND METHODS FOR MANUFACTURING SUCH MICROELECTRONIC ASSEMBLIES**

Declaration of Jason L. Fuller and Shaun D. Compton Under 37 C.F.R. § 1.131

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

We, Jason L. Fuller and Shaun D. Compton, declare and state that:

1. We are the joint inventors of the invention described and claimed in U.S. Patent Application No. 10/081,624 (the "present application") filed February 20, 2002. This declaration establishes invention in this country before April 10, 2001, and thus before the issue date of U.S. Patent No. 6,212,767.

2. Before April 10, 2001, we conceived the invention claimed in the present application. Our conception of the invention is corroborated by (a) the signed and redacted pages of Micron Technology, Inc. Invention Disclosure Form 01-0427 (hereinafter, the "01-0427 Disclosure," attached to this declaration as Exhibit A), and (b)

a signed and redacted page of Jason Fuller's Lab Book (hereinafter, the "Lab Book," attached to this declaration as Exhibit B).

3. As shown in the 01-0427 Disclosure and the Lab Book, we conceived of a method for assembling microelectronic dies. (See Exhibit A, pp. 1-2; and Exhibit B.)

4. In one embodiment set forth in claim 1, a method for assembling microelectronic dies includes placing a base die on a substrate in a first die attach head of a die attach machine so that a front side of the base die with bond pads faces toward the substrate and a backside of the base die faces away from the substrate. (See Exhibit A, page 1; and Exhibit B.) The method further includes stacking a first stacked die onto the backside of the base die in a second head of the same die attach machine by dispensing an adhesive onto the backside of the base die and placing a backside of the first stacked die onto the adhesive. (See Exhibit A, page 1; and Exhibit B.) Therefore, the first stacked die is stacked onto the base die before securing the base die to the substrate in a heating cycle. (See Exhibit A, page 1; and Exhibit B.)

5. We also conceived of another embodiment, as set forth in claim 2, wherein the method for assembling microelectronic dies further includes heating the based die and the first stacked die in a single heating cycle to secure the base die to the substrate and to secure the first stacked die to the base die. (See Exhibit A, pp. 1-2; and Exhibit B.)

6. We also conceived of another embodiment, as set forth in claim 7, wherein the method for assembling microelectronic dies further includes automatically transferring the substrate and the base die from the first die attach head to the second die attach head. (See Exhibit A, pp. 1-2.)

7. We also conceived of another embodiment, as set forth in claim 8, wherein the method for assembling microelectronic dies further includes transferring the substrate and the base die from the first die attach head to the second die attach head

without loading the substrate and the base die into a separate die attach machine. (See Exhibit A, pp. 1-2.)

8. We also conceived of another embodiment, as set forth in claim 9, wherein the method for assembling microelectronic dies further includes placing the base die on the substrate and stacking the first stacked die onto the base die in a single pass through a single die attach machine. (See Exhibit A, pp. 1-2.)

9. In yet another embodiment set forth in claim 10, a method for assembling microelectronic dies includes preparing a substrate to receive a base die in a first die attach head of a die attach machine, and placing the base die on the substrate in the first die attach head so that a front side of the base die with bond pads faces toward the substrate and a backside of the base die faces away from the substrate. (See Exhibit A, page 1; and Exhibit B.) The method further includes moving the base die to a second die attach head of the same die attach machine without heating the base die, and stacking a first stacked die onto the base die in the second die attach head by dispensing an adhesive onto the backside of the base die and placing the first stacked die onto the adhesive in the second die attach head. (See Exhibit A, page 1; and Exhibit B.)

10. We also conceived of another embodiment, as set forth in claim 11, wherein the method for assembling microelectronic dies further includes heating the base die and the first stacked die in a single heating cycle to secure the base die to the substrate and to secure the first stacked die to the base die. (See Exhibit A, pp. 1-2; and Exhibit B.)

11. After conceiving this invention, we proceeded diligently by preparing the 01-0427 Disclosure with our employer, working through a initial invention review procedure, participating in patent preparation activities with Paul Parker, and participating in other aspects of preparing the present patent application. On February 20, 2002, we constructively reduced this invention to practice with the filing of the present application.

12. We further declare that all statements herein made of our own knowledge are true, and that statements made on information or belief are believed to be true; and further, that the statements are made with the knowledge that the making of willful or false statements or the like is punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from this patent application.

_____
Jason L. Fuller

_____
Date

Residence	:	City of Meridian, County of Ada State of Idaho
Citizenship	:	United States of America
P.O. Address	:	1287 E. Drucker Street Meridian, Idaho 83642

Shaun D. Compton

8 Feb 2005
Date

Residence	:	City of Boise, County of Ada State of Idaho
Citizenship	:	United States of America
P.O. Address	:	2950 Raindrop Drive Boise, Idaho 83706

12. We further declare that all statements herein made of our own knowledge are true, and that statements made on information or belief are believed to be true; and further, that the statements are made with the knowledge that the making of willful or false statements or the like is punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from this patent application.

Jason L. Fuller

2-9-2005
Date

Residence	:	City of Meridian, County of Ada State of Idaho
Citizenship	:	United States of America
P.O. Address	:	2396 S. Ice Bear Court Meridian, Idaho 83642

Shaun D. Compton

Date

Residence	:	City of Boise, County of Ada State of Idaho
Citizenship	:	United States of America
P.O. Address	:	2950 Raindrop Drive Boise, Idaho 83706

Express Mail No. EV522678945US

Attorney Docket No. 108298636US
Disclosure No. 01-0427.00/US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:	JASON L. FULLER AND SHAUN D. COMPTON	EXAMINER:	JOHN T. HARAN
APPLICATION NO.:	10/081,624	ART UNIT:	1733
FILED:	FEBRUARY 20, 2002	CONF. NO:	1950
FOR:	**MICROELECTRONIC DEVICE HAVING A PLURALITY OF STACKED DIES AND METHODS FOR MANUFACTURING SUCH MICROELECTRONIC ASSEMBLIES**		

Declaration of Jason L. Fuller and Shaun D. Compton
Under 37 C.F.R. § 1.131

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Exhibit A

INVENTION DISCLOSURE 01-0427

1. INVENTOR(S):

Jason L Fuller
Shaun D Compton

2. DESCRIPTION:

- **Title:**

Method for processing a stacked FCIP (Flip Chip & Conventional in 1 pkg.)

- **Brief Description:**

Method includes the following in order: (1)Placing a flip chip component on the substrate (2)Dispensing epoxy on the backside of the flip chip (3)Placing another die into the epoxy (face up) on the back side of the flip chip. This process will only require one pass through the die attach machine. The substrate then indexes into the oven for solder reflow and epoxy snap cure at the same time. Another method would include utilizing a heated bond head to reflow the flip chip during placement. The flip chip die would then be mechanically attached during dispensing and placing the conventional die.

3. CONCEPTION & DOCUMENTATION OF INVENTION:

- **Date when first conceived:**

- **To whom was the idea first described:**

none

- **On what date:**

- **Date of the first tangible record:**

- **Type and location:**

Logged concept into Inventors Notebook.

4. INFORMATION RELATED TO INVENTION:

- **Related invention disclosures:**

I'm sure many stacked die disclosures exist, however, I don't know the details of any related to this concept. There is Micron internal documentation which depicts this titles "Conventional/FCIP Stack"

dated December The method for processing is undefined as far as I know.

- **Closest technology:**

  A two pass process where the flip chip is reflowed, and then ran through die attach a second time to apply the conventional (2nd) die.

- **Advantages of this invention over previous technology:**

  This would only require one pass through a die attach machine which increases output and simplifies the process.

5. **IMPORTANT DATES:**

   - **If the invention has been disclosed outside the company, please specify to whom it has been disclosed, when, and in what form:**

     No disclosures outside Micron

   - **If any articles describing your invention have been published, please specify the author(s), title of article, publication and date:**

     Don't know of such publications

   - **If any engineering samples have been given out, please specify to whom and on what date they were given:**

     N/A

   - **If any product using the invention has been sold or offered for sale, please specify to whom and on what date:**

     N/A

6. **DISPOSITION OF THE INVENTION:**

   - **When will (or did) Micron begin use of the invention experimentally:**

     Experiments will begin the week of

   - **When will (or did) Micron begin production of this invention:**

     No production to date. Applications are on the roadmap for late

7. **MISCELLANEOUS INFORMATION:**

   - **ARPA project:**

   - **Was the invention developed during a joint development agreement or other contract with an outside company:**

     No

- List developmental work outside of the company, including Government proposal or contract:

N/A

8. INVENTORS:

- _____

Name : Jason L Fuller
Home Address : 1287 E. Drucker
City : Meridian State : ID Zipcode : 83642
Citizenship : USA
Company : Micron Technology, Inc.
Work Phone # : 368-2669 Mail Stop : 906
Dept Name : Assembly Die Attach Dept # : 224
Supervisor : Ed Schrock
Signature : _____ Date :

- _____

Name : Shaun D Compton
Home Address : 1651 S. Riverstone Lane #202
City : Boise State : ID Zipcode : 83706
Citizenship : US
Company : Micron Technology, Inc.
Work Phone # : 363-1999 Mail Stop : 906
Dept Name : Assembly Dept # : 224
Supervisor : Ed Schrock
Signature : _____ Date : ___ ___ ___

9. WITNESS:

If there is only one (1) inventor, a witness should sign and date this disclosure. A witness in this case is a non-inventor who understands the nature of the invention.

_____ _____/_____/_____
(Signature of Witness) (Date)

Attorney Docket No. 108298636US
Disclosure No. 01-0427.00/US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:	JASON L. FULLER AND SHAUN D. COMPTON	EXAMINER:	JOHN T. HARAN
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Declaration of Jason L. Fuller and Shaun D. Compton Under 37 C.F.R. § 1.131

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Exhibit B

Notebook # 0101014

Project Number | Subject | Date

"FLUX APPLICATION FOR PROCESSING FLIP CHIP COMPONENTS"

DURING MY LAST TRIP TO JAPAN, IT OCCURRED TO ME THAT IT MAY BE POSSIBLE TO INCORPORATE A PIN TRANSFER PROCESS ON OUR EXISTING DIE ATTACH EQUIPMENT.

UNITIVE PRE-MEETING

DESIGN GUIDANCE FOR UNITIVE & FCT NEED TO BE REVIEWED - (KOSMUS)

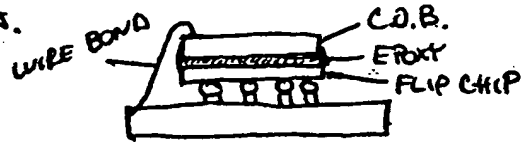
PROCESS OVERVIEW

1.) INTRODUCTIONS → MICRON ROADMAP
2.) UNITIVE PRESENTATION
- ORGANIZATION CHANGES / COMPANY STATUS
- TECHNOLOGY PRESENTATION (EXCLUSION RNG / PREFORMS)
- ROADMAP UTOB (TEST STRUCTURE)
- MANUFACTURING OVERVIEW

3.) QUESTIONAIRE RESPONSE CLARIFICATIONS
4.) QUESTIONS & ANSWER.

1 - NO ENTRIES SAVE — DUE TO EQUIP. PROCUREMENT (JP)

STACKED FLIP CHIP IN PACKAGE. A METHOD FOR STACKING A FLIP CHIP AND A C.O.B INTO THE SAME PACKAGE. THE FIRST DIE IS FLIP CHIP. EPOXY PASTE IS THEN DISPENSED ONTO THE BACKSIDE OF THE FLIP CHIP. THE C.O.B DIE IS THEN PLACED (FACE UP) INTO THE EPOXY PASTE. THIS PROCESS IS COMPLETED PRIOR TO SOLDER REFLOW. THE DIE ARE THEN PUT INTO THE SOLDER REFLOW OVEN AT THE SAME TIME WHICH SNAP CURES THE EPOXY AND REFLOWS THE SOLDER BUMPS.



(JP)

FOLLOWING POST CURE, THE C.O.B. DIE IS WIRE BONDED TO COMPLETE THE ELECTRICAL CONNECTION.

Author's Signature: _____ Date: _____

Witness' Signature: _____ Date: _____
(Read and Understood)

Please do not write in the margin

Express Mail No. EV551885914US

Attorney Docket No. 108298636US
Disclosure No. 01-0427.00/US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:	JASON L. FULLER AND SHAUN D. COMPTON
APPLICATION NO.:	10/081,624
FILED:	FEBRUARY 20, 2002
FOR:	**MICROELECTRONIC DEVICE HAVING A PLURALITY OF STACKED DIES AND METHODS FOR MANUFACTURING SUCH MICROELECTRONIC ASSEMBLIES**

EXAMINER:	JOHN T. HARAN
ART UNIT:	1733
CONF. NO:	1950

Declaration of David T. Dutcher Under 37 C.F.R. §1.132 to Establish Diligence

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

I, David T. Dutcher, do hereby declare:

1. The facts set forth in this Declaration are personally known to me based on (a) the time records of the law firm of Perkins Coie, LLP ("Perkins Coie") (hereinafter, the "Time Records," a redacted copy of which is attached to this Declaration as Exhibit A), and (b) the signed pages of Micron Technology, Inc. Invention Disclosure Form 01-0427 (hereinafter, the "01-0427 Disclosure," a copy of which is attached to this Declaration as Exhibit B).

2. I am an attorney at Perkins Coie, located at 1201 Third Avenue, Suite 4800, Seattle, Washington 98101, and I am outside patent counsel for Micron Technology, Inc. ("Micron").

3. On March 26, 2003, Jason L. Fuller and Shaun D. Compton, the joint inventors of the present application, signed the 01-0427 Disclosure.

4. On April 30, 2001, Micron's in-house patent legal department received the 01-0427 Disclosure from the inventors.

5. Between April 30, 2001 and July 24, 2001, Micron's Patent Committee reviewed and analyzed the 01-0427 Disclosure with regard to pursuing patent protection.

6. On July 24, 2001, the 01-0427 Disclosure was mailed to Perkins Coie.

7. Between July 24, 2001 and September 19, 2001, Paul Parker, an attorney at Perkins Coie, had a reasonable backlog of unrelated cases which he took up in chronological order and carried out expeditiously.

8. On September 19, 2001, Paul Parker reviewed the 01-0427 Disclosure and prepared and sent correspondence to J. Webster, a patent assistant at Micron, to set up an interview with the inventors.

9. On September 26, 2001, Paul Parker prepared correspondence to J. Webster and held a telephone conference with J. Webster regarding interviewing the inventors.

10. On October 4, 2001, Paul Parker prepared for an invention disclosure meeting with the inventors.

11. On October 5, 2001, Paul Parker held an invention disclosure meeting with the inventors, and prepared notes regarding same after the meeting.

12. On November 7, 2001, Paul Parker reviewed the 01-0427 Disclosure and prepared claims.

13. On November 8, 2001, Paul Parker further prepared claims, informal figures, and a draft of the specification.

14. On November 13, 2001, Paul Parker further prepared the claims, the background section, and the informal figures.

15. On November 14, 2001, Paul Parker further prepared the specification of the application.

16. On November 15, 2001, Paul Parker revised and edited a draft of the application, and prepared additional description of embodiments of the invention.

17. On November 19, 2001, Paul Parker further prepared the application.

18. On November 20, 2001, Paul Parker revised and edited the application.

19. On November 29, 2001, Paul Parker proofed the final edits to the application.

20. On November 30, 2001, Paul Parker proofed the drawings and the application.

21. On December 3, 2001, Rena Iov, a paralegal at Perkins Coie, prepared correspondence to forward the first draft of the application to the inventors.

22. Between December 3, 2001 and December 27, 2001, Jason L. Fuller and Shaun D. Compton (the inventors) reviewed the first draft of the application.

23. On December 27, 2001, Micron mailed the first draft of the application with the inventors' comments to Perkins Coie.

24. On January 7, 2002, Paul Parker reviewed the comments from the inventors and revised the application.

25. On January 19, 2002, Paul Parker proofed the edits to the application.

26. On January 22, 2002, Paul Parker finalized revisions to the second draft of the application.

27. On January 22, 2002, Rena Iov mailed the second draft of the application to the inventors.

28. Between January 22, 2002 and February 20, 2002, Jason L. Fuller and Shaun D. Compton (the inventors) reviewed the second draft of the application.

29. On February 20, 2002, Paul Parker reviewed and signed the documents to file the present application with the U.S. Patent and Trademark Office.

30. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that the making of willfully false statements and the like is punishable by fine, or imprisonment, or both, under Section 101 of Title 18 of the United States Code.

Respectfully submitted,
Perkins Coie LLP

Date: 9/19/05

David T. Dutcher
Registration No. 51,638

Correspondence Address:
Customer No. 25096
Perkins Coie LLP
P.O. Box 1247
Seattle, Washington 98111-1247
Phone: (206) 359-8000

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:	JASON L. FULLER AND SHAUN D. COMPTON
APPLICATION NO.:	10/081,624
FILED:	FEBRUARY 20, 2002
FOR:	**MICROELECTRONIC DEVICE HAVING A PLURALITY OF STACKED DIES AND METHODS FOR MANUFACTURING SUCH MICROELECTRONIC ASSEMBLIES**

EXAMINER:	JOHN T. HARAN
ART UNIT:	1733
CONF. NO:	1950

Declaration of David T. Dutcher Under 37 C.F.R. § 1.132 to Establish Diligence

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Exhibit A

Perkins Coie | PCNet

Important Note: You need to look carefully at the status code on this page. For time entries with a "P" (prebill) status, the "Billed Amount" reflects the matter value of time on the prebill. Such time has not yet been billed to the client. Only time entries with a "B" status have actually been billed to the client.

Time Detail

additional search criteria: Beginning Date:**Inception** Ending Date: **9/9/2005** Status: **'W','P','B'**

CSL: Parker, Paul T.

Client/Matter: 10829 Micron Technology, Inc. 8636.US00 Method for Processing a Stacked FCIP (FI

Time ID	Tkpr ID	Tkpr Name	Date	Base Hours	Billed Hours	Status	Invoice	Base Amount	Billed Amount	Phase/ Task
7204246	08821	Parker, Paul T.	9/19/2001							

Narrative: Review disclosure regarding interviewing inventors; prepare and send correspondence to J. Webster to set up interviews;

7221505	08821	Parker, Paul T.	9/26/2001							

Narrative: Prepare correspondence to J. Webster and telephone conference with J. Webster regarding interviewing inventors;

7238050	08821	Parker, Paul T.	10/4/2001							

Narrative: Prepare for meeting at Micron regarding disclosure of invention;

7237717	08821	Parker, Paul T.	10/5/2001							

Narrative: Disclosure conference with inventors regarding explaining invention and alternate embodiments; prepare notes regarding same after conference;

7323419	08821	Parker, Paul T.	11/7/2001							

Narrative: Review disclosure and prepare claims;

7325838	08821	Parker, Paul T.	11/8/2001							

Narrative: Further prepare claims; prepare informal figures; prepare draft of specification;

7340922	08821	Parker, Paul T.	11/13/2001							

Narrative: Further prepare claims; prepare background and informal figures;

7340944	08821	Parker, Paul T.	11/14/2001							

Narrative: Further prepare specification regarding application;

7340969	08821	Parker, Paul T.	11/15/2001							

Narrative: Revise and edit draft of application; prepare additional description of embodiments of the invention;

7359521	08821	Parker, Paul T.	11/19/2001							

Narrative: Further prepare application;

7359522 08821 Parker, Paul T. 11/20/2001

Narrative: Revise and edit application;

7379032 08821 Parker, Paul T. 11/29/2001

Narrative: Proof final edits to applications;

7379033 08821 Parker, Paul T. 11/30/2001

Narrative: Proof drawings and application;

7372334 08867 Iov, Rena 12/3/2001

Narrative: First draft of application; prepare Declaration; prepare Assignment; prepare Election and Power of Attorney; prepare Nonpublication Request; prepare application cover sheets; correspondence to client enclosing and forwarding same for review and signature;

7468368 08821 Parker, Paul T. 1/7/2002

Narrative: Review comments from inventors and revise application;

7490857 08821 Parker, Paul T. 1/19/2002

Narrative: Proof edits to application;

7505423 08821 Parker, Paul T. 1/22/2002

Narrative: Final revisions and send out second draft of application to client;

7485605 08867 Iov, Rena 1/22/2002

Narrative: Second draft of application; prepare application cover sheets; prepare redlined pages; correspondence to client enclosing application along with Declaration, Assignment, Election and Power of Attorney and Nonpublication Request;

7571191 08867 Iov, Rena 2/20/2002

Narrative: Final application; prepare PTO/SB/05; count claims and calculate fees; prepare General Authorization and Fee Transmittal; prepare drawing labels; prepare Form PTO-1595 for Assignment recordation; prepare filing fee check; prepare return receipt postcard; file all of same in the U.S. Patent and Trademark Office;

7580329 08821 Parker, Paul T. 2/20/2002

Narrative: Review and sign documents regarding filing application in PTO;

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF:	JASON L. FULLER AND SHAUN D. COMPTON
APPLICATION NO.:	10/081,624
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Mail Stop Amendment
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P.O. Box 1450
Alexandria, VA 22313-1450

Exhibit B

INVENTION DISCLOSURE 01-0427

1. INVENTOR(S):

Jason L Fuller
Shaun D Compton

2. DESCRIPTION:

- **Title:**

  Method for processing a stacked FCIP (Flip Chip & Conventional in 1 pkg.)

- **Brief Description:**

  Method includes the following in order: (1)Placing a flip chip component on the substrate (2)Dispensing epoxy on the backside of the flip chip (3)Placing another die into the epoxy (face up) on the back side of the flip chip. This process will only require one pass through the die attach machine. The substrate then indexes into the oven for solder reflow and epoxy snap cure at the same time. Another method would include utilizing a heated bond head to reflow the flip chip during placement. The flip chip die would then be mechanically attached during dispensing and placing the conventional die.

3. CONCEPTION & DOCUMENTATION OF INVENTION:

- **Date when first conceived:**

  03/01/2001

- **To whom was the idea first described:**

  none

- **On what date:**

- **Date of the first tangible record:**

  03/13/2001

- **Type and location:**

  Logged concept into Inventors Notebook.

4. INFORMATION RELATED TO INVENTION:

- **Related invention disclosures:**

  I'm sure many stacked die disclosures exist, however, I don't know the details of any related to this concept. There is Micron internal documentation which depicts this titles "Conventional/FCIP Stack"

dated December 2000. The method for processing is undefined as far as I know.

- **Closest technology:**

  A two pass process where the flip chip is reflowed, and then ran through die attach a second time to apply the conventional (2nd) die.

- **Advantages of this invention over previous technology:**

  This would only require one pass through a die attach machine which increases output and simplifies the process.

5. IMPORTANT DATES:

- **If the invention has been disclosed outside the company, please specify to whom it has been disclosed, when, and in what form:**

  No disclosures outside Micron

- **If any articles describing your invention have been published, please specify the author(s), title of article, publication and date:**

  Don't know of such publications

- **If any engineering samples have been given out, please specify to whom and on what date they were given:**

  N/A

- **If any product using the invention has been sold or offered for sale, please specify to whom and on what date:**

  N/A

6. DISPOSITION OF THE INVENTION:

- **When will (or did) Micron begin use of the invention experimentally:**

  Experiments will begin the week of 04/09/2001.

- **When will (or did) Micron begin production of this invention:**

  No production to date. Applications are on the roadmap for late 2001.

7. MISCELLANEOUS INFORMATION:

- **ARPA project:**

- **Was the invention developed during a joint development agreement or other contract with an outside company:**

  No

- **List developmental work outside of the company, including Government proposal or contract:**

  N/A

8. INVENTORS:

- ---

  Name : Jason L Fuller
  Home Address : 1287 E. Drucker
  City : Meridian **State** : ID **Zipcode** : 83642
  Citizenship : USA
  Company : Micron Technology, Inc.
  Work Phone # : 368-2669 **Mail Stop** : 906
  Dept Name : Assembly Die Attach **Dept #** : 224
  Supervisor : Ed Schrock
  Signature : _____ **Date** : 3/26/2001

- ---

  Name : Shaun D Compton
  Home Address : 1651 S. Riverstone Lane #202
  City : Boise **State** : ID **Zipcode** : 83706
  Citizenship : US
  Company : Micron Technology, Inc.
  Work Phone # : 363-1999 **Mail Stop** : 906
  Dept Name : Assembly **Dept #** : 224
  Supervisor : Ed Schrock
  Signature : _____ **Date** : 3/26/2001

9. WITNESS:

If there is only one (1) inventor, a witness should sign and date this disclosure. A witness in this case is a non-inventor who understands the nature of the invention.

_____ ____/____/____
(Signature of Witness) (Date)